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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,611	01/28/2004	Travis E. Swanson	DB001096-000	3432
57694	7590	05/14/2009	EXAMINER	
JONES DAY			CHUNG, PHUNG M	
222 East 41st Street				
New York, NY 10017-6702			ART UNIT	PAPER NUMBER
			2117	
			MAIL DATE	DELIVERY MODE
			05/14/2009	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/766,611	<b>Applicant(s)</b> SWANSON ET AL.	
	<b>Examiner</b> Phung M. Chung	<b>Art Unit</b> 2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2009.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-7 and 9-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-25 is/are allowed.
- 6) ☒ Claim(s) 1,2,4,5,7 and 9 is/are rejected.
- 7) ☒ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-2, 4-5, 7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lambrecht et al (6,035,364) in view of Swanson (6,292,911).

As per claim 1, Lambrecht et al disclose a method of providing a signaling pattern for a bus (on-chip bus 230) having a plurality of bit lines (first data bit line and second data bit line), said method comprising:

for each selected bit line in said plurality of bit lines,

selecting a first group (assign the first stream of data) of at least one of a plurality of signals to be sent over said selected bit line (first one or more data bit lines of the on-chip bus);

further selecting a second group (assign the second stream of data) of at least one of said plurality of signals to be sent over at least one bit line in said plurality of bit lines other than said selected bit line (a second one or more data bit lines of the on-chip bus) said selecting and said further selecting being performed by a memory controller;

transmitting said first group of signals on said selected bit line; and

transmitting said second group of signals over said at least one bit line in said plurality of bit lines other than said selected bit line. (See Fig. 4, col. 9, line 65-67 to col. 10, lines 1-15 and lines 60-67). Lambrecht et al do not specifically disclose that the generated data bits are pseudo-randomly generated bits, and a memory controller. However, Swanson discloses generated data bits are pseudo-randomly generated bits, and a memory controller (10). (See col. 6, lines 30-52). Therefore, it would have been obvious to a person of ordinary skilled in the art, at the time the invention was made, to incorporate the generated data bits that are pseudo-randomly generated bits as taught by Swanson into the generator of Lambrecht et al in order to ensure that some or all of those error producing bit patterns are tested, random or pseudo-random test patterns are selected.

As per claim 2, Lambrecht et al further disclose wherein said selecting is performed simultaneously with said further selecting. (See col. 10, lines 3-16 and lines 60-63).

As per claim 4, Swanson further discloses a test circuit 19 includes a duplicate test pattern generator so that a duplicate bit pattern is generated within memory (col. 5, lines 65-67 to col. 6, lines 1-3). Therefore, base on the teaching of a duplicate test

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pattern generator as taught by Swanson a person of skilled in the test art, at the time the invention was made, would sent each signal over said selected bit line that is identical to each responding signal sent over said at least one bit line in said plurality of bit lines other than said selected bit line so that it can be determined if the received test pattern has been corrupted.

As per claim 5, Swanson further discloses wherein the number of bit lines in said plurality of bit lines is  $2N$ , where  $N \geq 1$ . (See col. 5, lines 10-24).

As per claim 7, this method claim is rejected under similar rationale as set forth in claim 1.

As per claim 8, this method claim is rejected under similar rationale as set forth in claim 4.

3. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 10-25 are allowable.

5. Applicant's arguments with respect to claims 1-24-7 and 9-25 have been considered but are moot in view of the new ground(s) of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung M. Chung whose telephone number is (571)272-3818. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Beausoliel Robert can be reached on 571-272-3645. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Phung M. Chung/  
Primary Examiner  
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